REMARKS

Claims 1-20 are presented for further examination. Claim 1 has been amended. Claims 9-20 are new.

In the Office Action mailed October 4, 2004, the Examiner objected to the disclosure because the reference to the parent application should be corrected to state that the previous application is now U.S. Patent No. 6,383,905 B2. Applicant has amended the specification as requested by the Examiner.

Turning to the merits, claims 1-7 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,554,566 ("Lur et al."). Claims 1-6 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,893,751 ("Jenq et al."). Claim 8 was rejected under 35 U.S.C. § 103(a) as unpatentable over Lur et al. in view of U.S. Patent No. 5,654,589 ("Huang et al.").

Applicant respectfully disagrees with the bases for the rejections and requests reconsideration and further examination of the claims.

Claim 1 of the present application is directed to an integrated semiconductor device that comprises semiconductor material substrate having a polysilicon line with micro-rough indentations on a top surface portion formed by chemical mechanical polishing using a slurry solution having particles of a maximum size of less than one-half of the width of a polysilicon line. Claim 1 further recites the silicide film covering the micro-top surface portion of a polysilicon region. The micro-rough indentations on the top surface portion of the polysilicon line are ideally formed by particles in a slurry solution that are less than one-half the width of the polysilicon line. It has been found that this width of particle provides sufficient enhancement of surface area to reduce resistance, and particularly contact resistance with the polysilicon.

Jenq et al., U.S. Patent No. 5,893,751, is directed to a self-aligned silicide manufacturing method that treats gate terminal and source/drain diffusion regions with argon plasma or wet etching methods once or twice consecutively to increase the roughness of the polysilicon surfaces. Jenq et al. specifically teach at column 3, lines 14-20 that the wet etching method uses an etchant solution that is MSDS-PNE. While this method may increase surface roughness, it does not provide the level of roughness recited in claim 1 that is provided by

particles having a size no greater than one-half the width of the polysilicon line. This process parameter creates a final structural configuration that is not taught or suggested by Jenq et al.

Lur et al., U.S. Patent No. 5,554,566, by enhancing adhesion of a subsequent metal silicide by creating a wavy surface on the underlying polysilicon. Lur et al. teach at column 4, lines 22-47 several methods for creating the wavy surface on the polysilicon. The first method consists of subjecting the polysilicon to a bath of phosphoric acid. A second method consists of anodization in hydrofluoric acid. Lur et al. further describe yet a third method of native oxide stripping and annealing at a temperature between 550° to 650°C at a predetermined pressure. Nowhere do Lur et al. teach or suggest a micro-rough surface formed by particles having less than one-half the width of the polysilicon line. Moreover, the "wavy" surface of Lur et al. formed by the three methods described therein does not achieve the surface roughness and hence the increased adhesion provided by the structure of the present invention.

Huang et al., U.S. Patent No. 5,654,589, is directed to a landing pad technology doubled up as local interconnect and borderless contact for deep sub-half micrometer IC applications. Huang et al. has been cited by the Examiner for the description of a built-up multi-layer metallization. Nowhere do Huang et al. teach or suggest a micr-rough surface of a polysilicon line formed to have the structure recited in claim 1.

In view of the foregoing, applicant respectfully submits that claim 1 is allowable over Jenq et al. or Lur et al., taken alone or in any combination thereof.

Dependent claims 2-11 are directed to additional embodiments of the invention that are also distinguishable over the references cited and applied by the Examiner. For example, claim 5 is directed to a silicide film that comprises titanium silicide or titanium silicide/titanium nitride stack film. Claim 9 recites the width of the polysilicon line to be less than 0.1 μm. Claim 10 recites the silicide film formed to not enter a C-54 transformation phase, and claim 11 recites the film formed to enter a C-49 phase and not a C-54 phase. There is no teaching or suggestion in Jenq et al., Lur et al., or Huang et al., taken alone or in any combination thereof of any of these features in combination with claim 1. In view of the foregoing, applicant respectfully submits that claims 2-11 are clearly allowable.

New claims 12-20 are directed to various combination of the features described above, *i.e.*, a polysilicon line of less than 0.1 μm width having a micro-rough top surface formed

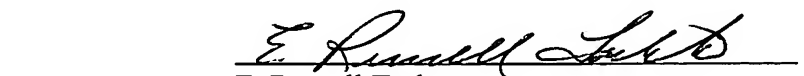
by a slurry solution using particles of a maximum size of less than one-half of a width of the polysilicon line, and a silicide film formed on the micro-rough top surface to enter a C-49 phase without entering a C-54 phase. As described more fully in the specification of the present invention, the C-49 phase presents a different structure than the C-54 phase which is obtained by annealing at a higher temperature. Avoiding the higher temperature required to enter the C-54 phase prevents damage to the structure, and the micro-rough surface enables entry into only the C-49 phase structure, thus avoiding the high temperature annealing and structural changes that take place when entering the C-54 transformation. Applicant submits that new claims 12-20 are allowable for these reasons as well as for the reasons discussed above with respect to claims 1-11.

In view of the foregoing, applicant submits that all of the claims in this application are clearly in condition for allowance. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicant's undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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